(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: 0 032 022 A1

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 80304583.0

(22) Date of filing: 18.12.80

(51) Int. Cl.³: H 01 L 21/265
H 01 L 21/76, H 01 L 21/74

(30) Priority: 21.12.79 JP 166596 79

(43) Date of publication of application:
15.07.81 Bulletin 81/28

(84) Designated Contracting States:
AT BE CH DE FR GB IT LI LU NL SE

(71) Applicant: FUJITSU LIMITED
1015, Kamikodanaka Nakahara-ku
Kawasaki-shi Kanagawa 211(JP)

(72) Inventor: Sakurai, Junji
7-11, Seta 4-chome Setagaya-ku
Tokyo 158(JP)

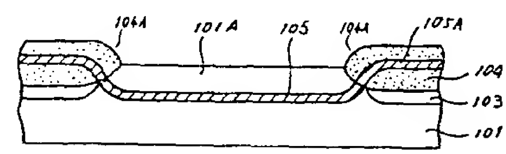
(72) Inventor: Kamioka, Hajime
370-40, Kamikashio-cho Totsuka-ku
Yokohama-shi Kanagawa 244(JP)

(74) Representative: Sunderland, James Harry et al.
HASELTINE LAKE & CO Hazlitt House 28 Southampton
Buildings Chancery Lane
London WC2A 1AT(GB)

(54) A semiconductor integrated circuit device and a method of fabricating such a device.

(57) An oxide layer 104 is formed on a semiconductor substrate 101 by selective oxidation. Thereby the edges 104A of a window in the oxide layer 104 have edges which are naturally tapered. Using the oxide layer 104 as a mask, a buried layer 105 is formed by ion implantation. The buried layer is flat at the centre of the window, curves up to the surface of the semiconductor substrate 101 in correspondence to the tapered edges 104A of the oxide layer 104 and extends into the oxide layer 104. A part of the buried layer 105B is exposed by etching of the oxide layer 104, and a contact region 110 is formed at that exposed part.

Fig. 9



EP 0 032 022 A1

 HL2189

A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND A METHOD OF FABRICATING SUCH A DEVICE.

The present invention relates to a semiconductor integrated circuit device and a method of fabricating such a device.

Conventionally, a transistor in a bipolar integrated circuit device has a structure as indicated in Figure 1 of the accompanying drawings which is a schematic cross-sectional diagram. In Figure 1, 1 is a P type semiconductor substrate; 2 is an N type epitaxial layer formed on the substrate 1; 3 is an N^+ type buried layer deposited at the boundary between substrate 1 and the epitaxial layer 2; 4 is a P type isolation region formed to extend to the substrate 1 from the surface of the epitaxial layer 2. In addition, 5 is a P type base region formed on or in the epitaxial layer 2 in a region defined within the isolation region 4 for the formation of an active element; 6 is an N^+ type emitter region formed within the base region 5; 7 is an N^+ type collector contact region formed within the epitaxial layer 2. Moreover, 8 is an insulating film covering the surface of the epitaxial layer 2; 9 is an emitter electrode; 10 is a base electrode; and 11 is a collector electrode.

In such a bipolar transistor, the collector of the transistor consists of the N^+ type buried layer 3 and the N^+ type collector contact region 7. Collector series resistance can be reduced and the operating speed characteristic can be improved (that is, operating

speed can be increased) by forming buried layer 3 and the collector contact region 7 in proximity to one another and, when possible, in such a way that they contact one another.

However, in a production method for fabricating the bipolar transistor of Figure 1, the collector contact region 7 is generally formed simultaneously with the emitter region 6 and as a result it is formed with almost the same depth as the emitter region 6 and does not extend down to the buried layer 3. As a result, the epitaxial layer 2 of lower impurity concentration extends between the collector contact region 7 and the buried layer 3, so that a reduction in collector series resistance is not achieved.

It has been attempted to form the collector contact region 7 more deeply by forming the emitter region 6 and the collector contact region 7 separately, but this results in an increase in the number of fabrication steps required.

In order to overcome such difficulties of forming a collector in a conventional bipolar transistor and in the fabrication methods for such formation, the present applicant has proposed the following method in Japanese Patent Application No. 50-364 (application date: December 23rd, 1974).

That is, as indicated in Figure 2 of the accompanying drawings, which is a schematic cross-sectional view, an insulating film 22 of silicon dioxide is formed to a thickness of about 1 μm on the surface of a P type silicon semiconductor substrate 21.

Then, as illustrated in Figure 3 of the accompanying drawings, which is another schematic cross-sectional view, parts of the insulating film 22 are selectively removed by etching, thus forming a window 23 in which a part of the semiconductor substrate 21 is exposed. The edge 23A of the window 23 in the insulating film 22 is provided with a taper of an inclination of about 45° by a proper selection of etching conditions.

Thereafter, phosphorus ions (P^+) are implanted into the semiconductor substrate 21 using the insulating film 22 as a mask, and thereby, as illustrated in Figure 4 of the accompanying drawings, which is another schematic cross-sectional diagram, an N^+ type buried layer 24 is formed. The N^+ type buried layer 24 is flat beneath the window 23 (that is, lies at a constant depth) but is inclined and changes continuously in depth at areas just under the inclined portions of the insulating film 22 and part of the buried layer 24 extends up to the boundary between the semiconductor substrate 21 and the insulating film 22.

Then, the insulating film 22 is removed, and as illustrated in Figure 5 of the accompanying drawings, which is another schematic cross-sectional diagram, an insulating film 25 is newly formed on the surface of the semiconductor substrate 21.

Thereafter, a window is provided in the insulating film 25, and phosphorus ions (P^+) are implanted into a P type region 26 which is surrounded by the N^+ type layer 24 and into an exposed area of the N^+ type buried layer 24, and thereby, as illustrated in Figure 6 of the accompanying drawings, which is another schematic cross-sectional diagram, an N^+ type emitter region 27 and an N^+ type collector contact region 28 are formed. The P type region 26 provides a base region. In Figure 6, 29, 30 and 31 are respectively an emitter electrode, a base electrode and a collector electrode.

N^+ type buried layer 24 forms a collector region, and a part of that N^+ type buried layer is led up to the surface of the semiconductor substrate by means of only a single ion implantation step. Therefore, it is sufficient for the purposes of leading out the collector to a collector electrode, to form the collector contact region 28 to the same depth as the emitter region 27, and thereby the production process can be simplified as compared with that required for the realization of the

structure illustrated in Figure 1.

However, in the method illustrated in Figures 2 to 6, it is difficult to form a tapered portion with a desired inclination at the edge 23A of the window 23 on the insulating film 22 in the process illustrated in Figure 3. That is, after providing the window 23 on the insulating film 22, a tapered portion is formed at the edge 23A of the window 23 by changing the etching solution or by changing the mask used for etching, thus making the process of forming a window 23 with a desired inclination angle and size troublesome and difficult.

According to the present invention there is provided a method of fabricating a semiconductor circuit device, wherein an insulating layer is formed on the surface of a semiconductor substrate, which insulating layer is provided with a window having an edge which is tapered (which tapers down to the surface of the substrate) and a buried layer is formed in the substrate, using the insulating layer as a mask, in such a manner that the buried layer is flat at the centre of the window and turns up to the surface of the substrate towards the edge of the window.

According to the present invention there is also provided a semiconductor integrated circuit device comprising a semiconductor substrate, an insulating layer formed on a surface of the semiconductor substrate and having a window with the edge tapered for defining an active region, a buried layer which is flat at the centre of the window, and curves up to the surface of the semiconductor substrate adjacent the edge of the window, and a circuit element formed in the region surrounded by the buried layer and employing the buried layer as one conductive region thereof.

An embodiment of the present invention can provide a structure for an element having a buried layer, in a bipolar integrated circuit device, which facilitates the leadingout of the buried layer.

An embodiment of the present invention can provide

a structure for an element having a buried layer, in a bipolar integrated circuit device, such that integration density in the device can be improved.

An embodiment of the present invention can provide a method of fabrication of an element having a buried layer, in a bipolar integrated circuit device, which facilitates the leading out of the buried layer to the surface of a semiconductor substrate in which the element is formed.

An embodiment of the present invention can provide a method of fabrication of an element having a buried layer, in a bipolar integrated circuit device, whereby integration density can be improved.

The present invention can also be applied to I^2L semiconductor integrated circuit devices.

Briefly, an embodiment of the present invention provides a semiconductor integrated circuit device having a semiconductor substrate, an insulating layer formed on the surface of the semiconductor substrate, with a window therein, having inclined edges, for defining an active region of the semiconductor substrate, a buried layer which is flat below the centre of the active region of the semiconductor substrate and turns up to the surface of the semiconductor substrate with a certain curvature in areas below the edges of the window in the insulating layer, and a circuit element structured in the active region and surrounded by the buried layer which provides one conductive region of the element.

An embodiment of the present invention also provides a method of fabricating a semiconductor integrated circuit device comprising steps for:

forming an insulating layer having a window therein with tapered or inclined edges by selectively oxidizing the surface of a semiconductor substrate,

defining an active region within the window provided in the insulating layer,

implanting impurities, by ion implantation, into the

semiconductor substrate using the insulating layer as a mask,

thus to form an ion implanted layer which is formed at uniform depth in areas of the substrate not masked by the insulating layer, and which extends upwards to the surface of the semiconductor substrate in correspondence to the tapering edge portions of the insulating layer and moreover which extends continuously into the insulating layer from the surface of the semiconductor substrate,

exposing at least a part of the ion implanted layer at the surface of the semiconductor substrate by removing surface portions of the insulating layer, and

forming a circuit element, wherein the ion implanted layer is taken to be a buried layer, in the region of the semiconductor substrate surrounded by the ion implanted layer.

Reference is made, by way of example, to the accompanying drawings, in which:-

Figure 1 is a cross-sectional diagram illustrating the structure of a conventional bipolar transistor in a bipolar integrated circuit device;

Figures 2 to 6 are respective cross-sectional diagrams for assistance in explanation of a method of producing a bipolar transistor previously proposed by the present applicant;

Figures 7 to 13 are respective cross-sectional diagrams illustrating a first process for fabricating a bipolar integrated circuit device embodying the present invention; and

Figures 14 and 15 are respective cross-sectional diagrams, and Figure 16 is a plan view, illustrating a second process for fabricating a bipolar integrated circuit device , in this case an I^2L device, embodying the present invention.

Figures 7 to 13 illustrate a process embodying the present invention for fabricating a bipolar transistor in a bipolar integrated circuit device

embodying the present invention.

A P type silicon (Si) substrate 101 with an impurity concentration of about 1×10^{15} atoms/cm^3 is first prepared.

Next, a silicon nitride film 102 is selectively formed on an active region of the surface of the silicon substrate 101 (e.g. on a region where a circuit element is to be formed) and a channel cut layer 103 with a concentration (of impurity) as high as 1×10^{17} atoms/cm^3 is formed at the surface of silicon substrate 101 by ion implantation of boron ions (B^+) into the surface of the silicon substrate 101 using the silicon nitride film 102 as a mask. This is illustrated in Figure 7.

Thereafter, the surface of the silicon substrate 101 is oxidised using a selective oxidation process employing the silicon nitride film 102 as a mask and thereby a silicon dioxide film (SiO_2) layer 104 is formed to a thickness of about 1.1 μm. This is illustrated in Figure 8.

As a result of the selective oxidation process employing silicon nitride film 102 as a mask, the silicon dioxide layer 104 is formed in such a manner that a part of it progresses beneath the bottom of the silicon nitride film 102 along the boundary between the silicon nitride film 102 and the silicon substrate 101, causing the formation of a so-called "bird's beak". When the silicon nitride film 102 is removed, the exposed portion of the silicon substrate 101, namely the active region, is defined by andsurrounded by the silicon dioxide layer 104 of which the edge 104A is inclined or tapered or curved.

Thereafter, phosphorus ions (P^+) are implanted into the silicon substrate 101 using the silicon dioxide layer 104 as a mask. For example, the ion implantation conditions are as follows: acceleration energy 400 KeV, and dosage 1×10^{15} atoms/cm^2. As a result, as illustrated in Figure 9, an N^+ type buried layer of 2×10^{19} atoms/cm^3 is formed at a depth of 5000Å to 6000Å within the silicon

substrate 101 where the substrate 101 is not covered by the silicon dioxide layer 104, and an ion implantation layer 105A is formed at a depth of 4000Å to 4500Å within the silicon dioxide layer 104, and the N^+ type buried layer 105 and the ion implantation 105A come into contact with each other at the surface of the silicon substrate 101 beneath the tapered or inclined edge 104A of the silicon dioxide layer 104. Namely, the N^+ type buried layer 105 gradually approaches or curves up to or comes up close to the surface of the silicon substrate 101, in a fashion provided by the tapering angle or curvature of edge 104A, under the tapered edge 104A of the silicon dioxide layer 104 and appears at the surface of the silicon substrate 101 under the silicon dioxide layer 104.

An active region 101A of the silicon substrate 101 surrounded by the N^+ type buried layer 105 is inverted to an N^- type region with a surface impurity concentration of about 1×10^{17} atoms/cm^3 by such phosphorus ion implantation. Such inversion is effected because the phosphorus ions are normally distributed (Gaussian distribution) in the ion implanted region. When it is required to further increase impurity concentration of such N^- type active region 101A, this can be done by further implantation of phosphorus ions into the active region 101A by reducing ion implantation energy.

Thereafter, the surface of the silicon dioxide layer 104 is removed by etching using a fluoric acid series etching solution. As a result of the phosphorus ion implantation, parts beneath the surface of the damaged silicon dioxide layer to a depth of about 4000Å to 4500Å are easily etched. In addition, as a result of such etching process, the edge 105B of the N^+ type buried layer 105 is exposed. This is shown in Figure 10. In the etching of the silicon dioxide layer 104, the etching speed of parts which have been subjected to ion implantation is enhanced to about twice that of

parts not subjected to ion implantation. Therefore, termination of etching for parts which have been subject to ion implantation can be detected easily by observing etching speed changing points.

Thereafter, a silicon dioxide film 106 is formed to a thickness of about 2000Å by a thermal oxidation process on the surface of the active region 101A . Then a window is selectively provided on the silicon dioxide film 106 and/or boron ions are implanted using a photoresist layer (not illustrated) formed on the silicon dioxide film 106 as a mask, and thereby a P type base region 107 is formed on the active region 101A. For example, such boron ion implantation can be carried out under such condition that acceleration energy is 50 KeV and dose is 1×10^{15} atoms/cm^2. As a result, the base region 107 is formed to a thickness of about 1500Å. This is shown in Figure 11.

Windows are provided in the silico dioxide film 106 where it covers the base region 107 and where it covers exposed portion 105B of the N^+ type buried layer 105 and a phospho-silicate glass (PSG) layer 108 is then formed to a thickness of about 6000Å to 1 μm covering over the windows and silicon dioxide layer 104 and silicon dioxide layer 106. A well known CVD (chemical vapour depositon) method can be used for formation of PSG layer 108.

Then, phosphorus is diffused from the PSG layer 108 by heat treatment and thereby an N^+ type emitter region 109 and an N^+ type collector contact region 110 with a surface concentration of 1×10^{20} atoms/cm^3 and a depth of about 2000Å are formed.

The base region 107 reaches a depth of 3000Å because boron ions advance by diffusion. This is shown in Figure 12.

Next, windows are formed selectively on the PSG layer 108 and silicon dioxide film 106, and moreover an aluminium layer is deposited to a thickness of about 1 μm by an evaporation method covering the windows and PSG layer 108. In succession, the aluminium layer

is selectively removed by etching to form an emitter electrode 111, a base electrode 112, and a collector electrode 113. This is shown in Figure 13.

In the bipolar transistor structure indicated with reference to Figures 7 to 13, N^+ type buried layer 105 which forms a portion for leading out the collector extends up to the surface of the semiconductor substrate at curved end parts thereof, and thereby connection to collector contact region 110 can be effected easily;as a result collector region series resistance can be made very small.

Therefore, high speed operation can be realized by the bipolar transistor structure.

In addition, since the formation of the collector contact region 110 does not require the utilization of a wider area than necessary for other steps,a bipolar transistor structured as in Figures 7 to 12 can be made small in size, thus realising higher integration density in an integrated circuit device.

According to the embodiment of thepresent invention described above, since the silicon dioxide layer formed by a selective oxidation process is used as a mask for obtaining a buried layer, the edge of the window provided by the mask is naturally tapered or curved. Therefore, as compared with the previous proposal of Figures 2 to 6, the fabrication processes involved in an embodiment of the present invention are much simplified as compared with the prior method wherein the edge is provided with a taper through a plurality of processing steps for the edge of a window of the mask used for forming the buried layer.

Moreover, since,in the embodiment of the present invention illustrated above, the emitter region and collector contact region are formed in the same process step, fabrication steps can be simplified.

Furthermore, according to the embodiment of the present invention described above, the buried layer is formed by an ion implantation method and circuit elements

such as a transistor are formed in a part of the semiconductor substrate surrounded by the buried layer, so that an epitaxial layer forming process which is required in the prior proposal of Figure 1 is no longer necessary and thereby fabrication processes are simplified.

Figures 14 to 16 illustrate an Integrated Injection Logic (I^2L) device, and the fabrication of such a device, according to another embodiment of the present invention. The I^2L device is formed by using similar techniques to those described above in connection with Figures 7 to 13. Thus, a buried layer (203) can be formed which curves upwards .. towards the semiconductor substrate surface. The buried layer is formed using an oxide film (202), formed by selective oxidation, as a mask , so that curved or tapered edges of the oxide film are naturally provided.

Figure 14 shows that a silicon dioxide layer 202 having a tapered edge is grown on the surface of an N type silicon substrate 201 by a selective oxidation method and then N^+ type buried layers 203 are formed by phosphorus ion implantation using the silicon dioxide layer 202 as a mask.

Thereafter, P type regions 204A, 204B, 205A, 205B are formed by selective diffusion of boron or by boron ion implantation in the active regions surrounded by the N^+ type buried layers 203. Here, since the silicon dioxide layer 202 which is used as the mask for ion implantation is formed with a tapered edge, the N^+ type buried layers 203 rise to the surface of the silicon substrate 201 along the tapered edge.

The foregoing ion implantation for obtaining the buried layer 203 is performed under conditions, for example, such that acceleration energy is 400 KeV and the dosage 1×10^{15} atoms/cm^2. The ion implantation for obtaining the P type regions 204, 205 is performed under conditions, for example, such that acceleration energy is 50 KeV and the dosage is 1×10^{14}

atoms/cm^2.

Figure 15 illustrates that, after exposing parts of the N^+ type buried layers 203 by removing parts of the silicon dioxide layer 202 damaged by ion implantation by etching, a silicon dioxide film 206 is formed on the surface of the active region; N type regions 207A, 207B, 207C and 207D and 208A, 208B are formed by providing windows in the silicon dioxide film 206 and by implanting arsenic ions (As^+) into the P type regions 205A, 205B and N type region 201; and then electrodes are formed by providing windows in the silicon dioxide film 206 and depositing a metal layer such as aluminium and selectively removing parts of the metal layer.

The ion implantation of arsenic is carried out under conditions, for example, such that acceleration energy is 80 KeV and the dosage is 5×10^{15} atoms/cm^2.

Figure 16 shows a plan view of the I^2L device as illustrated in Figure 15.

In the structure shown in Figures 15 and 16, P type regions 204A, 204B,N type regions 201 and P type regions 205A, 205B form lateral PNP transistors within regions surrounded by the N^+ buried layer 203 with the P type regions 204A, 204B used as injectprs and N type regions 201 as base regions.

In addition, N type regions 201, P type regions 205A and 205B and N type regions 207A, 207B, 207C and 207D form vertical NPN transistors respectively for which the N^+ type buried layers 203 are used as emitter lead out portions, P type regions 205A and 205B are used as base regions and N type regions 207A, 207B, 207C and 207D are used as collector regions. Electrodes 209A, 209B are respective injector electrodes and electrode 210 is used as a base electrode of lateral PNP transistors and as emitter electrodes of vertical NPN transistors. Moreover, electrodes 211A, 211B are respectively used as collector electrodes of lateral PNP transistors and as

base electrodes of vertical NPN transistors. Thus, electrodes 212A to 212D form collector electrodes of the vertical NPN transistors.

In such a structure embodying the present invention, since N^+ type buried layers 203 extend up to the surface of the semiconductor substrate, connection between an emitter region and an emitter contact region 208 of a vertical NPN transistor can be made very easily and thereby emitter region series resistance can be kept very small.

Since an emitter region electrode is deposited at the surface of the silicon substrate 201, connection with a lead wire leading out the electrode can be easily effected.

Furthermore, since the P type injector regions 204A, 204B are surrounded by N^+ type buried layers 203 except for surfaces of the injector regions facing P type regions 205A, 205B, a lesser amount of carriers (holes) injected are lost and injection efficiency of the lateral PNP type transistors can be improved.

According to the embodiment of the present invention illustrated in Figures 14 to 16, since a silicon dioxide layer formed by a selective oxidation process is used as a mask for forming a buried layer 203, the required tapered portion is formed naturally at the edge of a window in the mask. For this reason the silicon dioxide layer is directly used as the mask and thereby a buried layer 203 of which the edge extends up to the surface of the silicon substrate 201 can be formed very easily.

Thus, an embodiment of the present invention provides a structure for a semiconductor integrated circuit device which includes circuit elements such as a bipolar transistor for example, in which a buried layer for the bipolar transistor is formed by an ion implantation method using an insulating layer formed with a window therein the edge of which window is tapered at the surface of a semiconductor substrate, as a mask. A part of the buried layer appears at the surface of the semiconductor

substrate, thus providing for establishment of connection to electrodes. Such a circuit element is formed in an active region surrounded by the buried layer.

The present invention provides a semiconductor integrated circuit device comprising; a semiconductor substrate, an insulating layer formed on a surface of said semiconductor substrate and having a window with the edge tapered for defining an active region, a buried layer which is flat at the centre of the active region of semiconductor substrate defined by said insulating layer and is extending up to the surface of said semiconductor substrate with the portion near the window of said insulating layer curved, and a circuit element structured in said active region with said buried layer considered as the one conductive region.

A semiconductor integrated circuit device comprising; a semiconductor substrate having one conductivity type, an insulating layer formed on a surface of said semiconductor substrate and having a window with the edge tapered for defining an active region, a buried layer of the opposite conductivity type which is flat the centre of the active region defined by said insulating layer and is extending up to the surface of said semiconductor substrate with the portion near the window of said insulating layer curved, the first region of the opposite conductivity type which is surrounded by said buried layer in said active region, a region of one conductivity type formed in said first region of the opposite conductivity type, the second region of the opposite conductivity type which is formed in said region one conductivity type, and a bipolar circuit element where said buried layer is used as the leading portion of said first region of opposite conductivity type.

A semiconductor integrated circuit device comprising; a semiconductor substrate of one conductivity type, an insulating layer formed on a surface of said semiconductor substrate and having a window with the edge

tapered for defining an active region, a buried layer of one conductivity type which is flat at the centre of the active region defined by said insulating layer and is extending up to the surface of said semiconductor substrate with the portion near the window of said insulating layer curved, the first region of one conductivity type surrounded by said buried layer in said element forming region, the first and second regions of opposite conductivity type being formed separately in a lateral direction within said first region of one conductivity type, the second region of one conductivity type formed within said first region of opposite conductivity type, and an integrated injection logic element where said buried layer is used as a leading out portion of said first region of one conductivity type.

A method for fabricating a semiconductor integrated circuit device comprising the steps for; forming the insulating layer having a window with the edge tapered by selectively oxidizing the surface of a semiconductor substrate, defining an active region by said window provided on said insulating layer, ion implanting impurities into said semiconductor substrate using said insulating layer as the mask, forming an ion implanted layer which is formed at the equal depth in the area not masked by said insulating layer, extending up to the surface of said semiconductor substrate corresponding to said tapering at the edge portion of said insulating layer and moreover extending continuously into said insulating layer from the surface of said semiconductor substrate, exposing at least a part of said ion implanted layer to the surface of said semiconductor substrate by removing the surface portion of said insulating layer, and forming a circuit element where said ion implanted layer is considered as the buried layer in the region of said semiconductor substrate surrounded by said ion implanted layer.

CLAIMS

1. A method of fabricating a semiconductor circuit device, wherein an insulating layer is formed on the surface of a semiconductor substrate, which insulating layer is provided with a window having an edge which is tapered (which tapers down to the surface of the substrate), and a buried layer is formed in the substrate, using the insulating layer as a mask, in such a manner that the buried layer is flat at the centre of the window and turns up to the surface of the substrate towards the edge of the window.

2. A method as claimed in claim 1, wherein the insulating layer is formed by selective oxidation of the surface of the substrate, thereby to provide the window with an edge which is tapered, and wherein the buried layer is formed in such a manner that it has a constant depth in a region of the substrate not masked by the insulating layer, turns up to the surface of the substrate in correspondence with the tapering of the edge of the window, and extends in a continuous manner into the insulating layer from the surface of the substrate.

3. A method as claimed in claim 1 or 2, wherein the buried layer is formed by ion implantation of impurities into the substrate and insulating layer.

4. A method as claimed in claim 1, 2 or 3, wherein a part of the buried layer is exposed by removing a portion of the insulating layer.

5. A method as claimed in claim 4, wherein a contact region is formed at the exposed part of the buried layer.

6. A method as claimed in any preceding claim, wherein a circuit element is formed in that part of the substrate above and surrounded by the buried layer.

7. A method as claimed in claim 6, wherein the circuit element is a bipolar element.

8. A method as claimed in claim 6, wherein the circuit element is an I^2L element.

9. A method as claimed in any one of claims 1 to 6, wherein the semiconductor substrate is of one conductivity

type and the buried layer is of the opposite conductivity type, and wherein a first region, of the said opposite conductivity type, is formed which is surrounded by the buried layer, a second region, of the said one conductivity type, is formed in the first region, a third region, of the said opposite conductivity type, is formed in the second region, and a bipolar circuit element is formed in which the buried layer is used as a lead out portion for the said first region.

10. A method as claimed in any one of claims 1 to 6, wherein the semiconductor substrate is of one conductivity type and the buried layer is of the said one conductivity type, and wherein a first region, of the said one conductivity type, is formed which is surrounded by the said buried layer, second and third regions, of the opposite conductivity type, are formed separately in a lateral direction within the first region, a fourth region, of the said one conductivity type, is formed within the said first region, and an integrated injecting logic element is formed in which the buried layer is used as a lead out portion for the first region.

11. A semiconductor circuit device fabricated by a method as claimed in any one of claims 1 to 10.

12. A semiconductor integrated circuit device comprising a semiconductor substrate, an insulating layer formed on a surface of the semiconductor substrate having a window therein the edge of which is tapered, and a buried layer which is flat at the centre of the window and curves up to the surface of the semiconductor substrate adjacent the edge of the window, and a circuit element formed in the region surrounded by the buried layer and employing the buried layer as one conductive region thereof.

13. A device as claimed in claim 12, wherein the insulating layer is formed by selective oxidation of the semiconductor substrate.

14. A device as claimed in claim 12 or 13, wherein a

contact region is formed at a part of the said buried layer at the surface of the semiconductor substrate.

Fig. 1

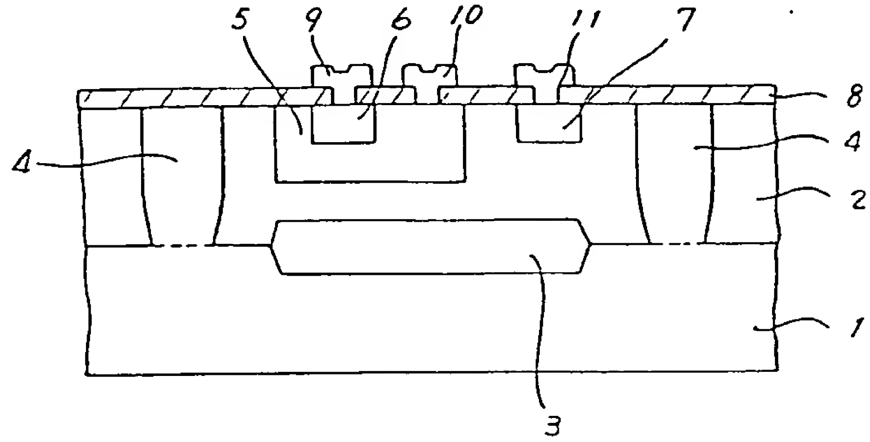


Fig. 2

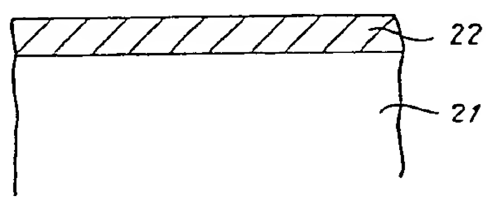


Fig. 3

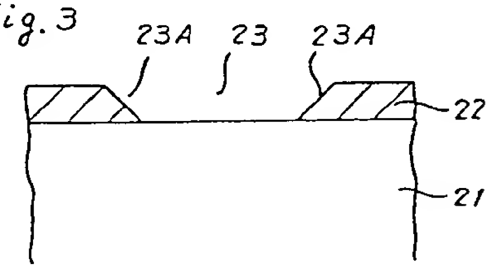


Fig. 4

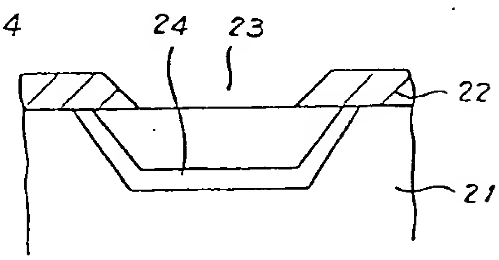


Fig. 5

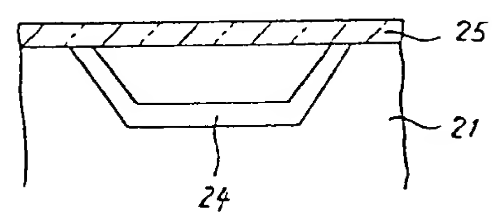


Fig. 6

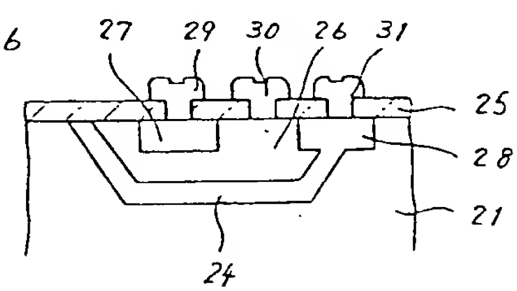


Fig. 7

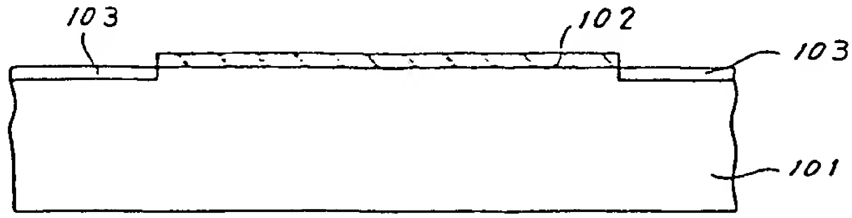


Fig. 8

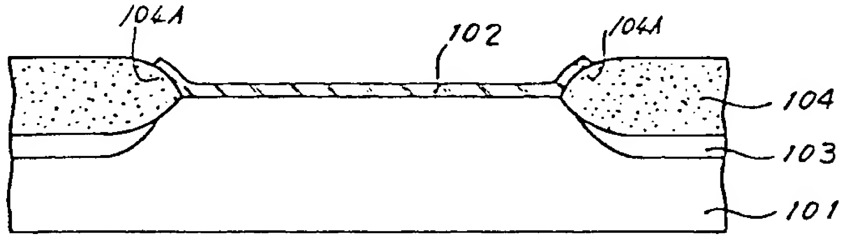


Fig. 9

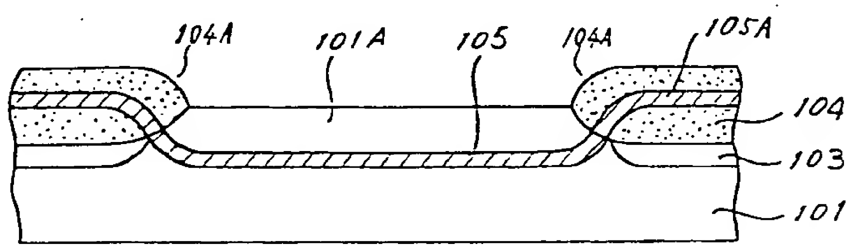


Fig. 10

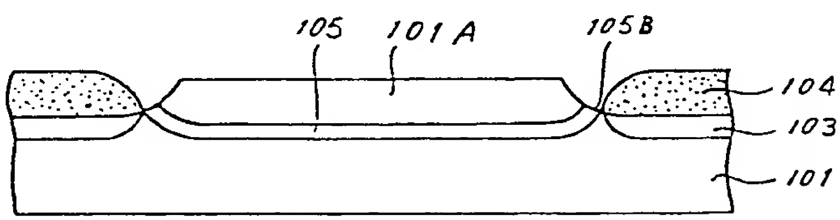


Fig. 11

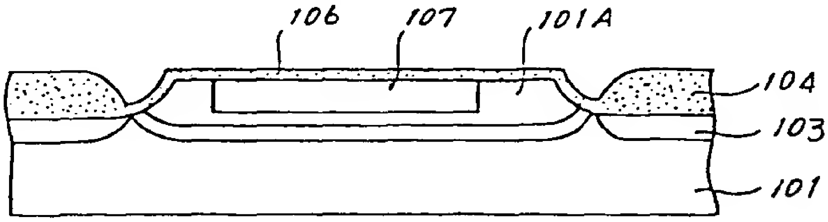


Fig. 12

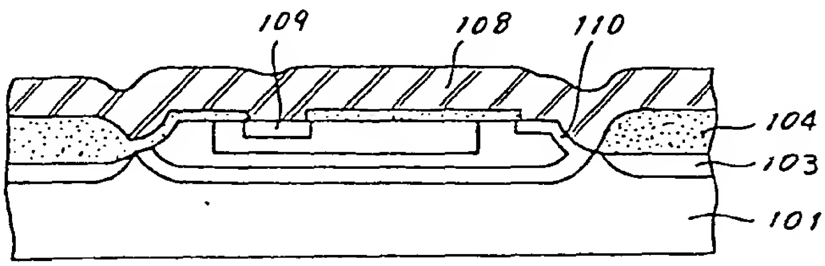


Fig. 13

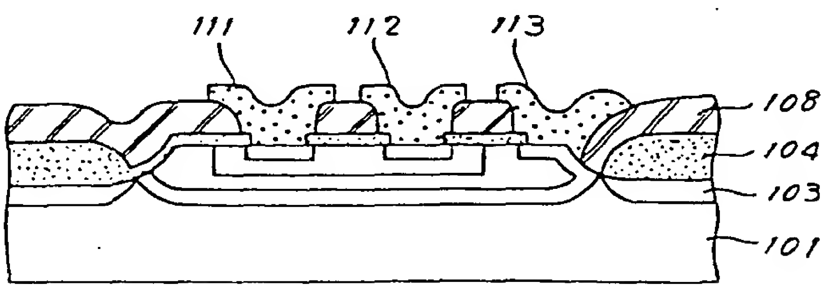


Fig. 14

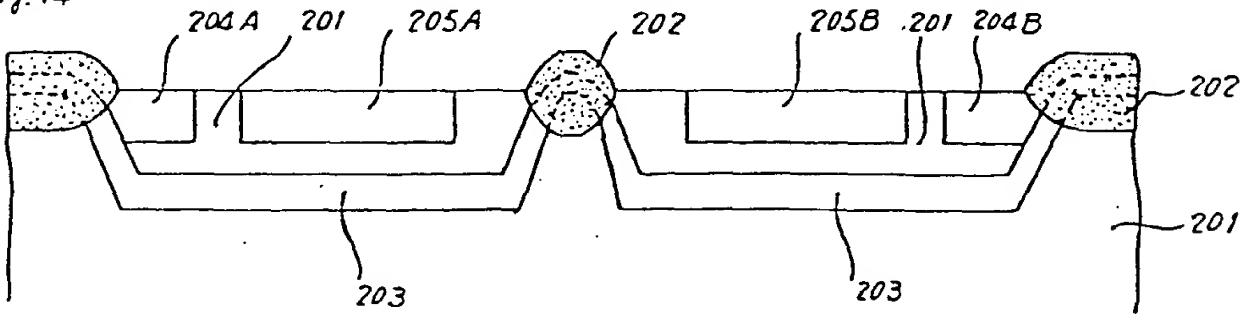


Fig. 15

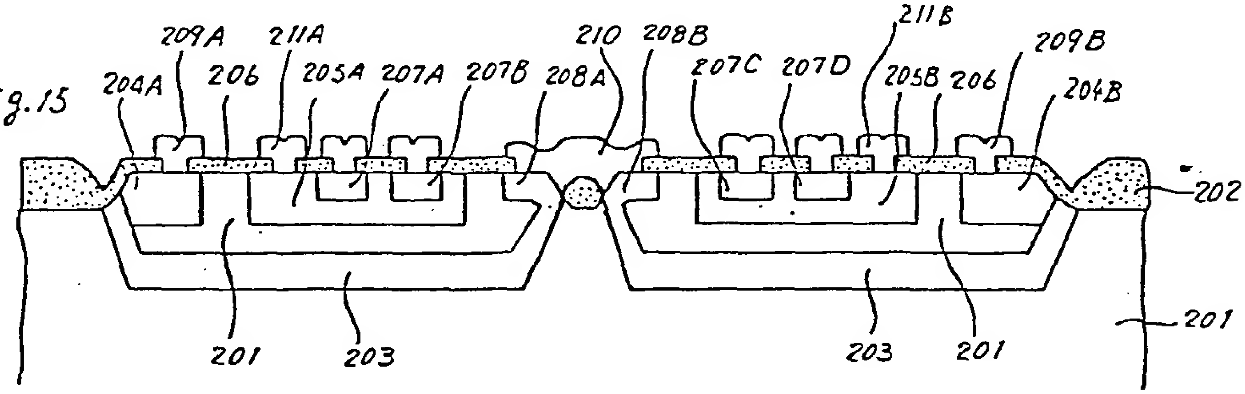
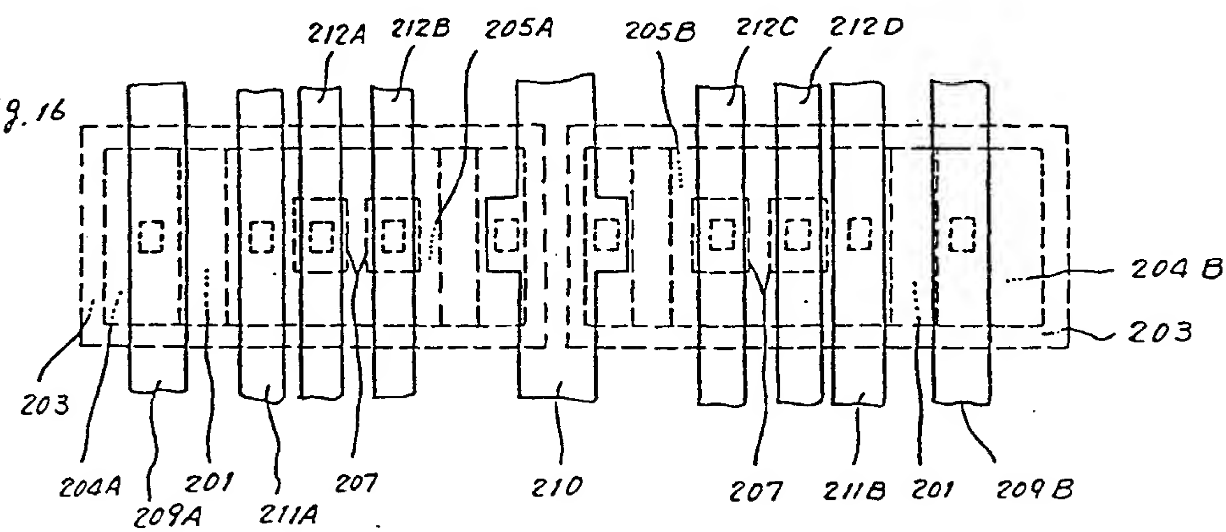


Fig. 16



0032022

European Patent Office

EUROPEAN SEARCH REPORT

Application number
EP 80 30 4583

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim
X	JP - A - 53 87672 (NIPPON DENKI K.K.) * Abstract and figures *	1-7,9, 11-14
X	NEWS AUS DER TECHNIK, volume 1978, no. 3, June 15, 1978, Wuerzburg, DE "Herstellung bipolarer integrierter Schaltungen ohne Epitaxie", abstract 465, * Abstract 465 and figures *	1-2, 5-6, 7-8, 10
X	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 19, no. 11, April 1977, New York, US A.E. MICHEL et al. "Bipolar integrated circuits without epitaxial layers", page 4151. * Page 4151, complete *	1-2, 5-8, 10
A	IBM TECHNICAL DISCLOSURE BULLETIN vol. 14, no. 5, October 1971, New York, US J.E. ZIEGLER et al. "Self-isolating bathtub collector for a planar transistor", pages 1635-1636. * Page 1636, complete and figures A and B *	1

CLASSIFICATION OF THE APPLICATION (Int. Cl.³)

H 01 L 21/265
21/76
21/74

TECHNICAL FIELDS SEARCHED (Int. Cl.³)

H 01 L 21/265
H 01 L 21/76
H 01 L 21/74

CATEGORY OF CITED DOCUMENTS

X: particularly relevant
A: technological background
O: non-written disclosure
P: intermediate document
T: theory or principle underlying the invention
E: conflicting application
D: document cited in the application
L: citation for other reasons

&: member of the same patent family, corresponding document

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	31-03-1981	FRANSEN

EPO Form 1503.1 06.78